



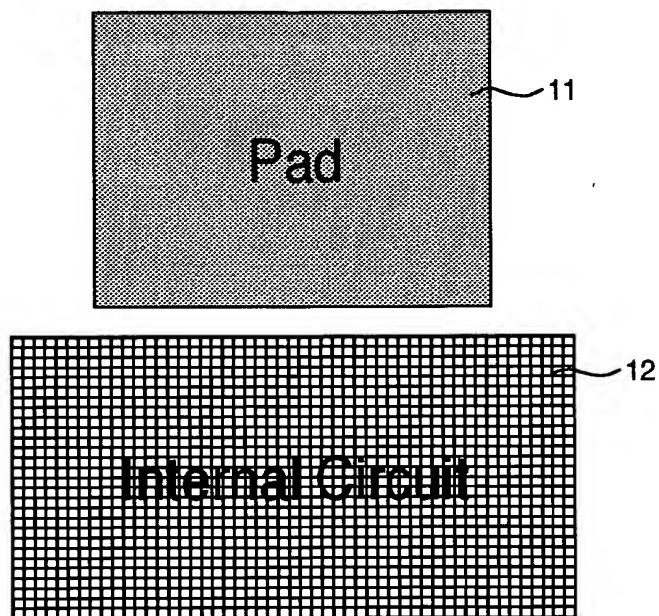
TITLE: IMPROVING ELECTROSTATIC DISCHARGE PERFORMANCE OF A SILICON STRUCTURE AND EFFICIENT USE OF AREA WITH ELECTROSTATIC DISCHARGE PROTECTIVE DEVICE UNDER THE PAD APPROACH AND ADJUSTMENT OF VIA CONFIGURATION THERETO TO CONTROL DRAIN JUNCTION RESISTANCE

INVENTOR(S): Nian Yang, Hiroyuki Ogawa, Yider Wu, Kuo-Tung Chang, and Yu Sun

USSN: 10/758,173 Attorney Docket #: AMD-AF01210

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Top side view

(Conventional Art)

Fig. 1

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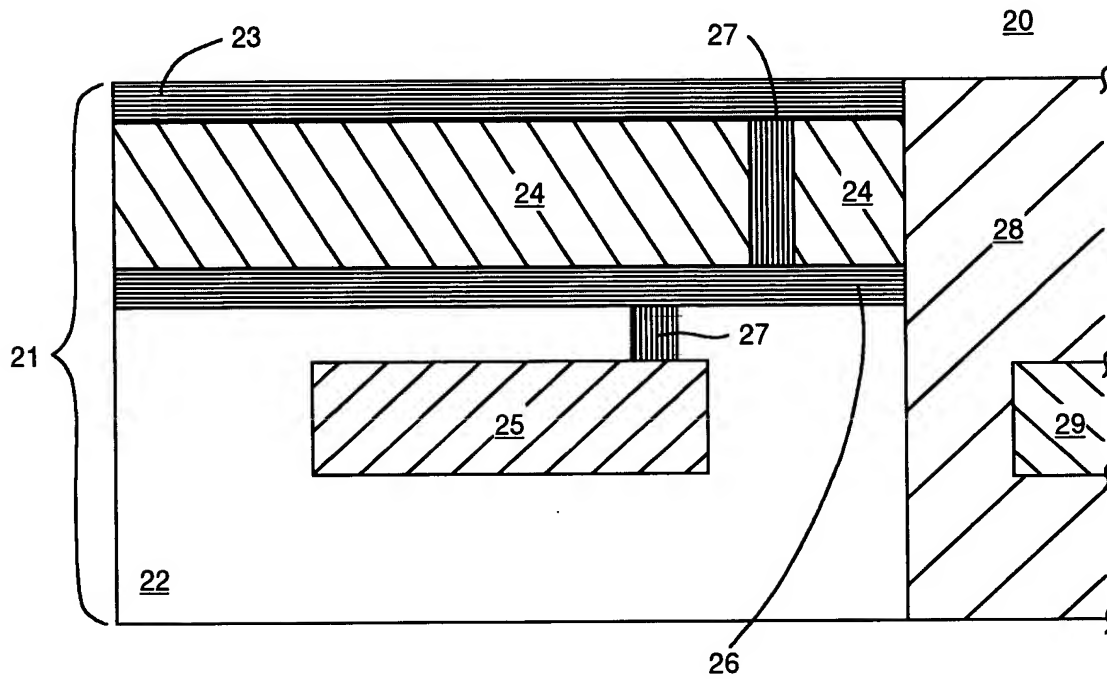


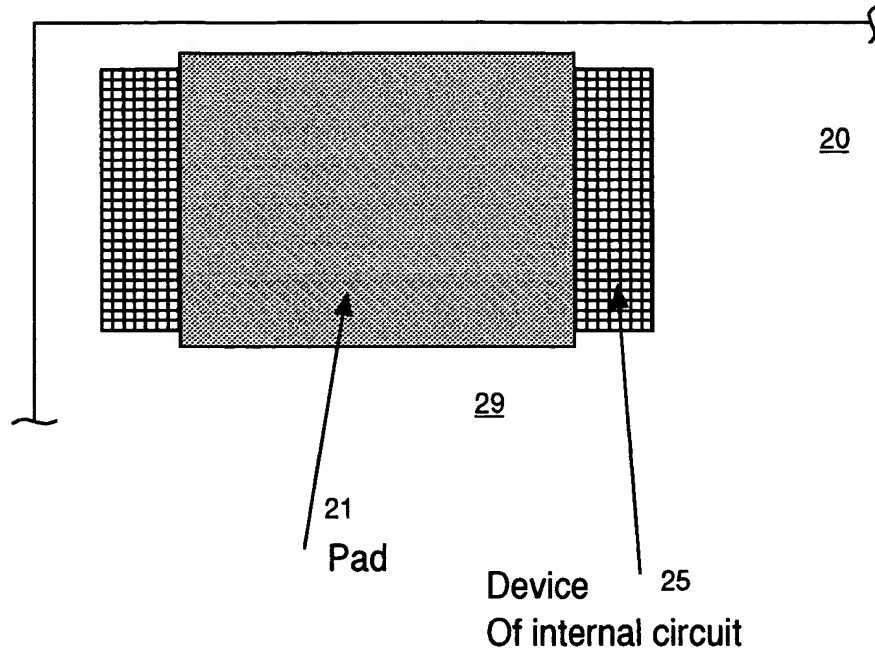
Fig. 2

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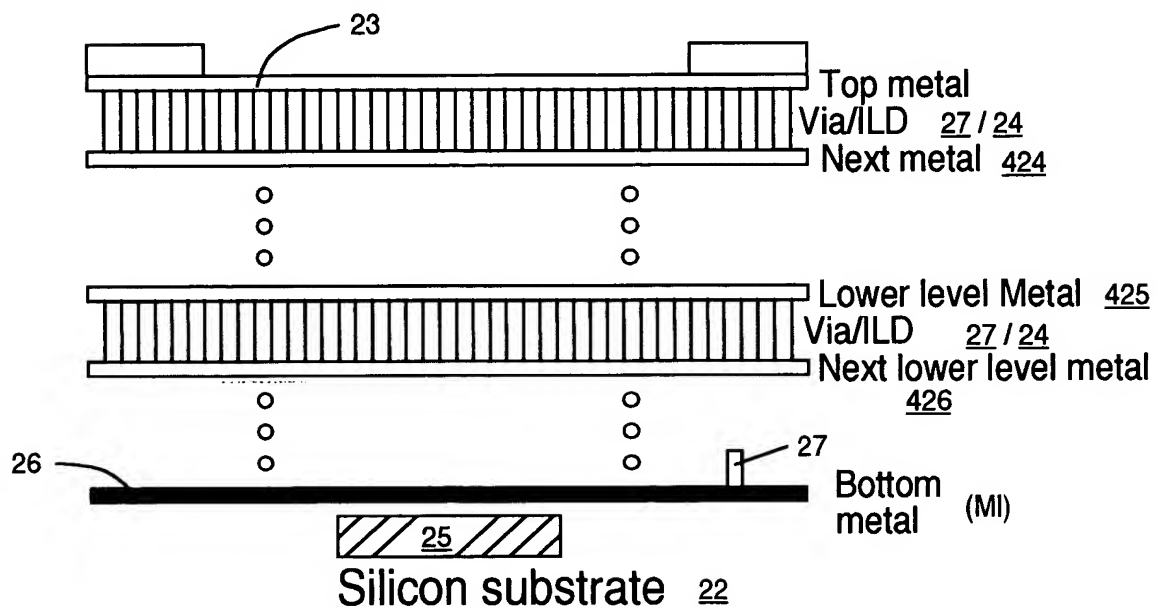
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Top side view

Fig. 3

400



Cross section view

Fig. 4

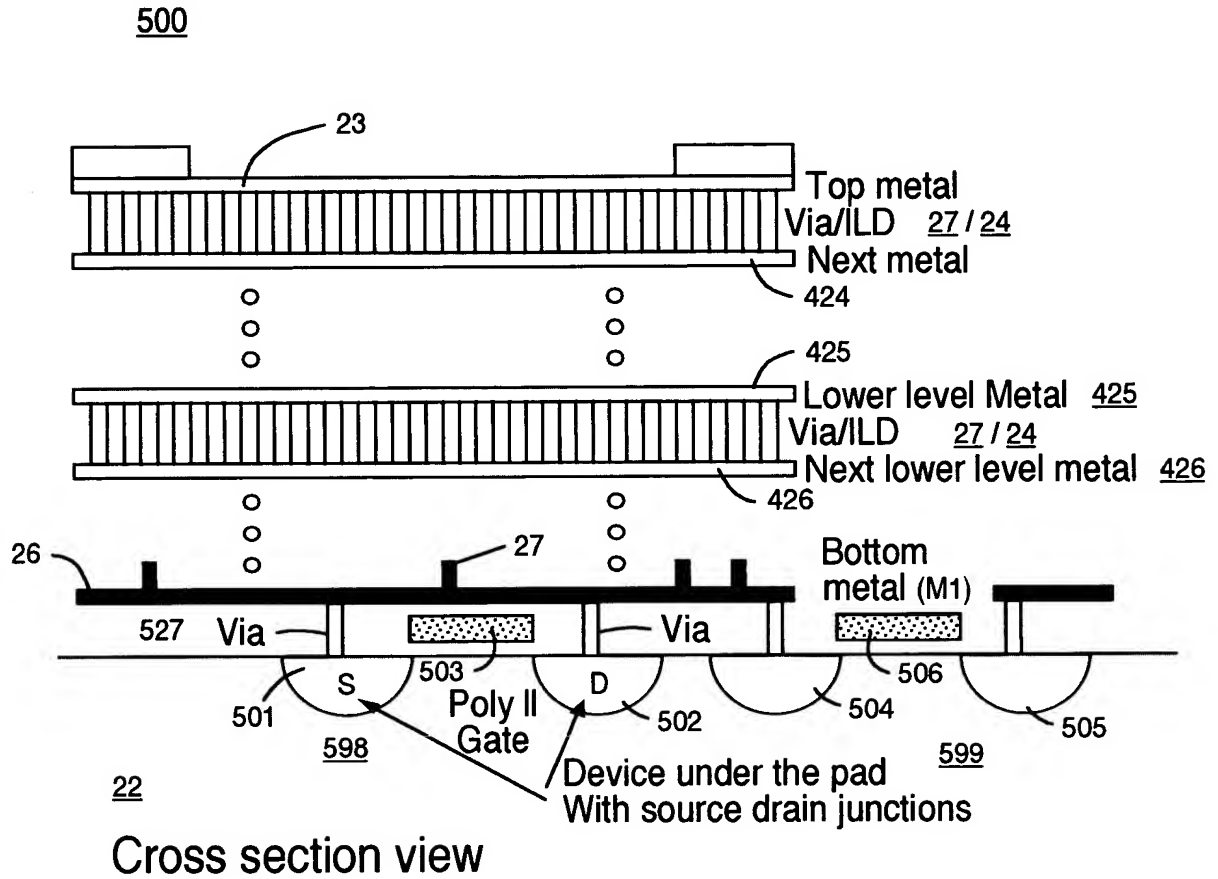


Fig. 5

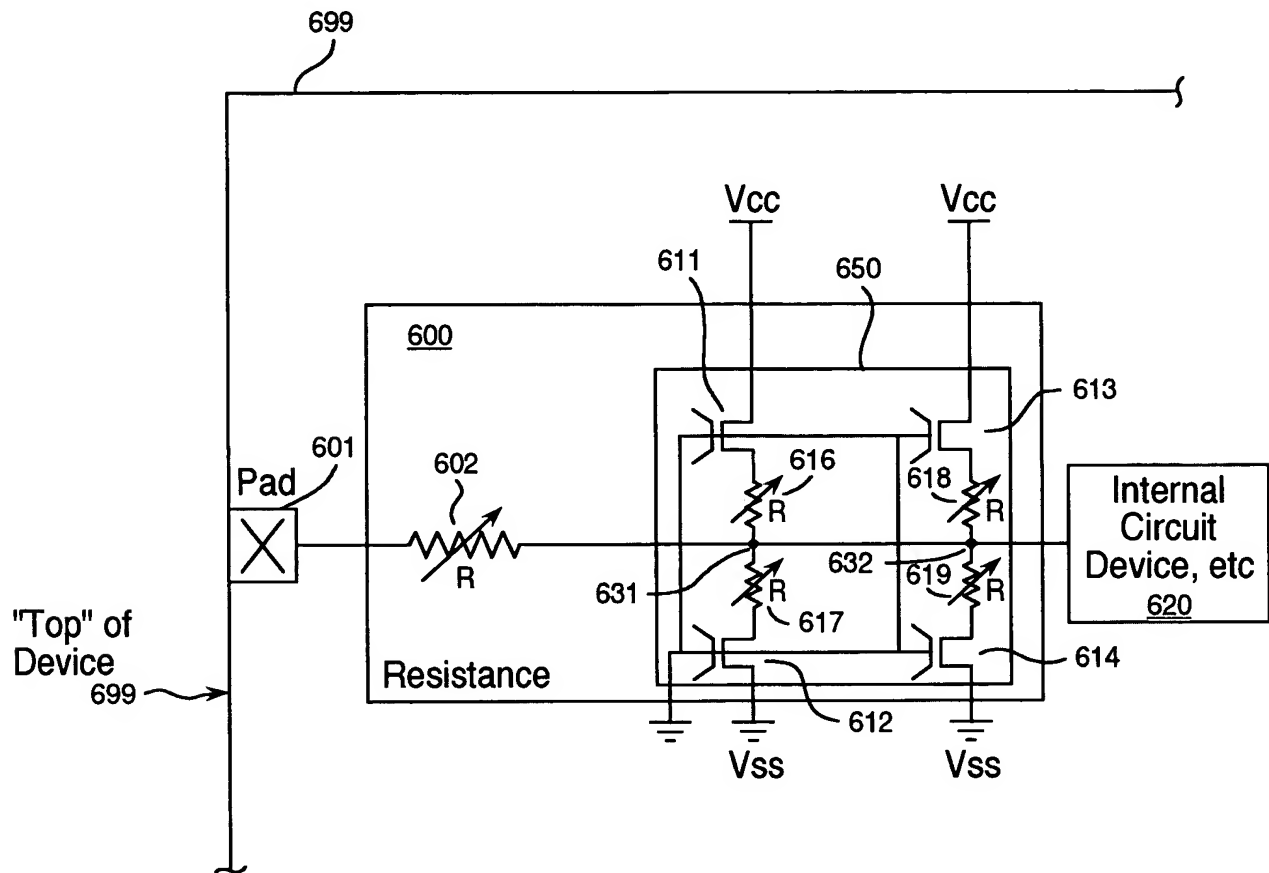


Fig. 6

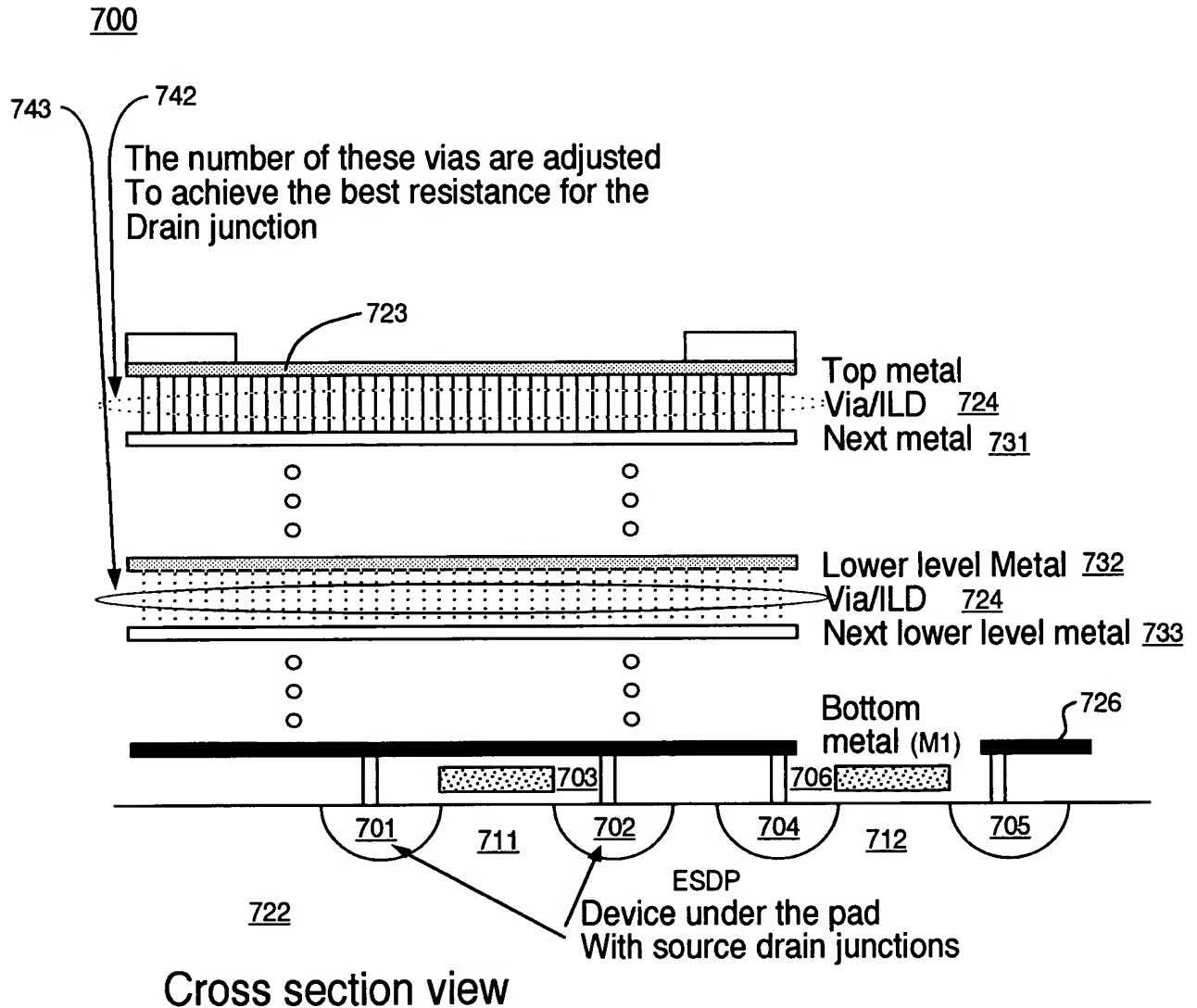


Fig. 7

80 Fabricating a Semiconductor Structure with ESD Protection

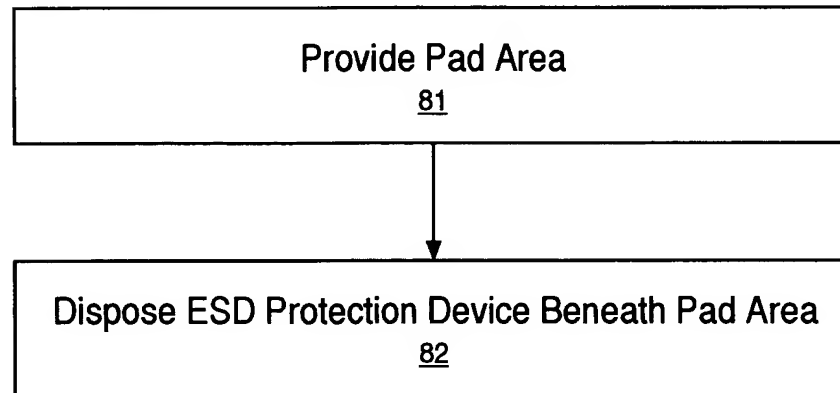


Fig. 8

90

Fabricating a Semiconductor Structure

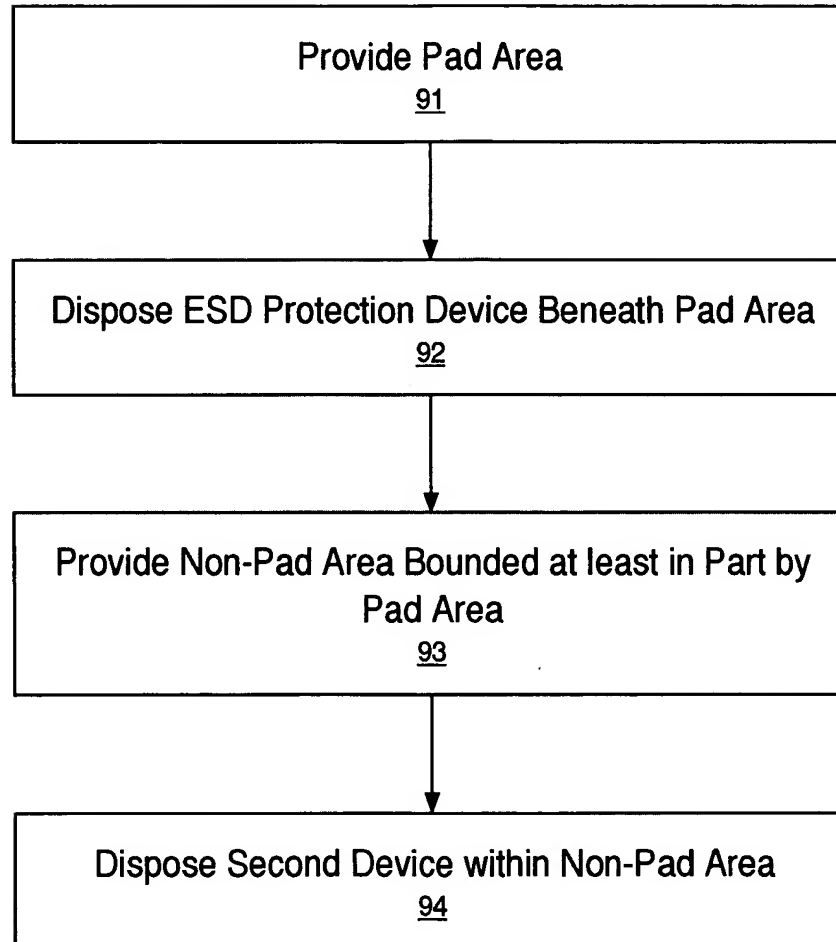


Fig. 9

100

Fabricating a Pad Area

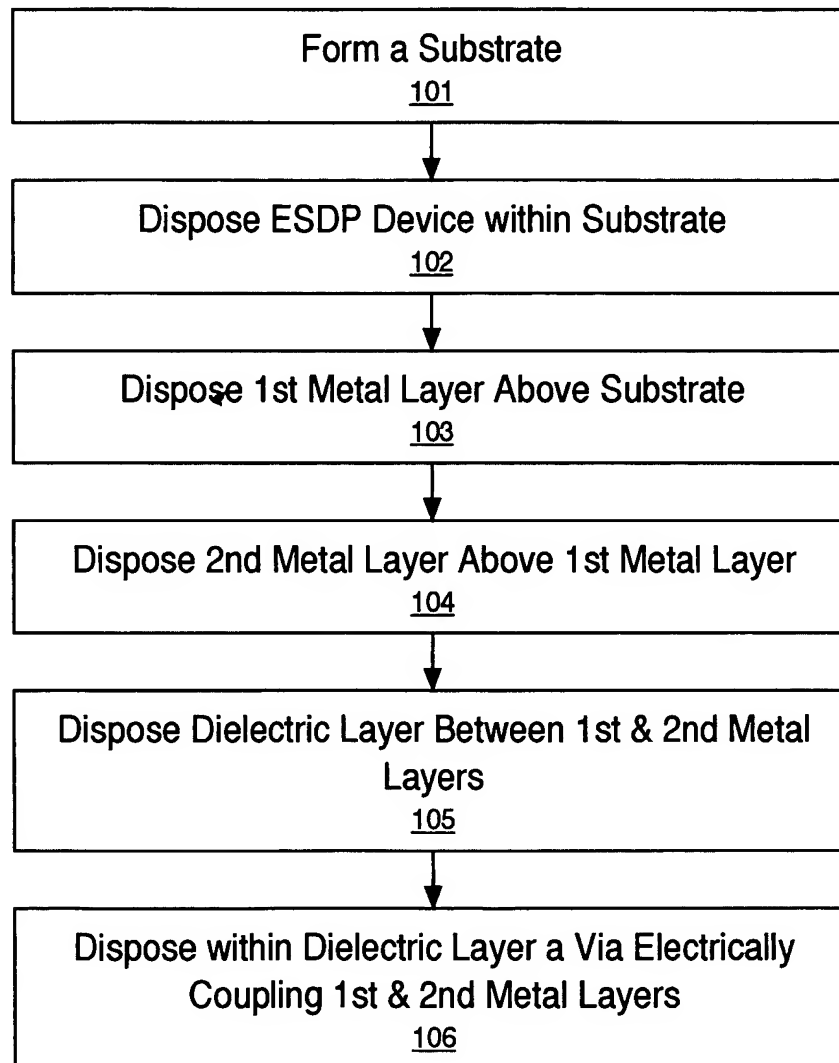


Fig. 10

1100 Fabricating a Pad Area with ESD Protection Device Below

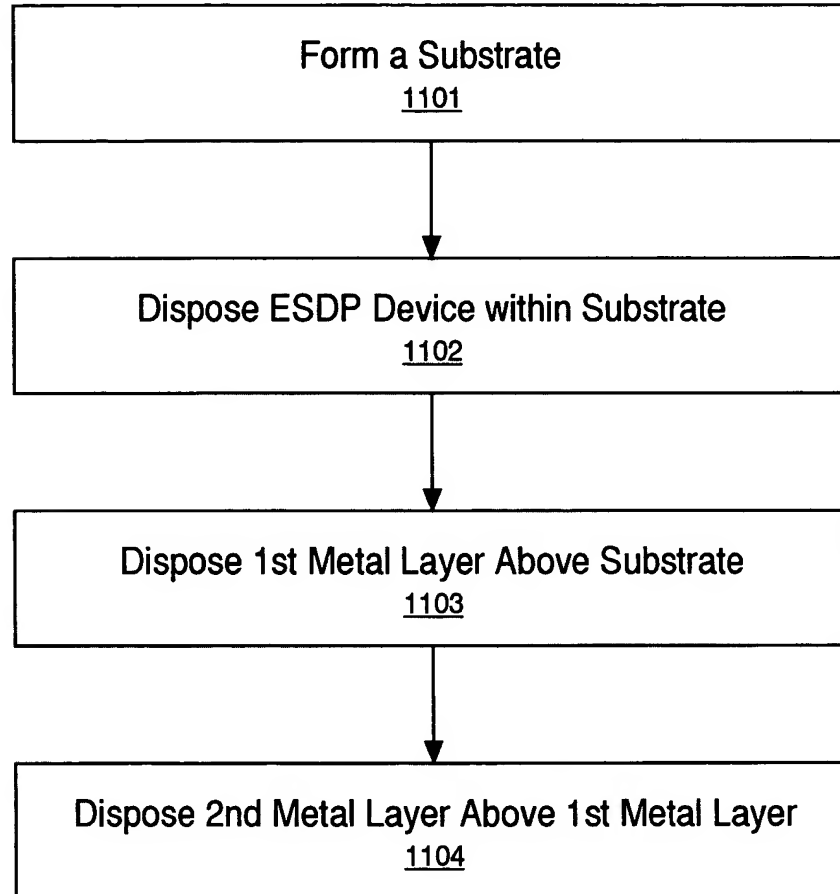


Fig. 11

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1200

Fabricating a Pad Area with ESDP Below

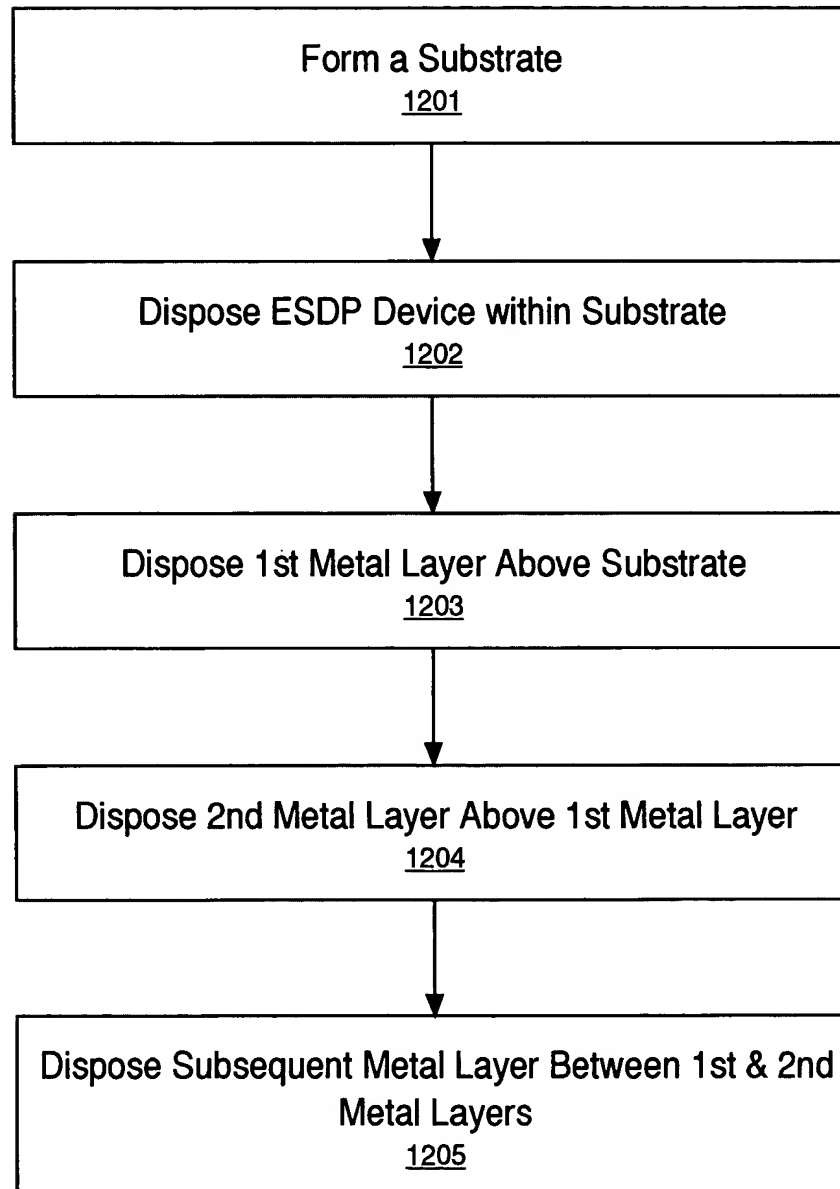


Fig. 12

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1300

Fabricating an ESDP Device

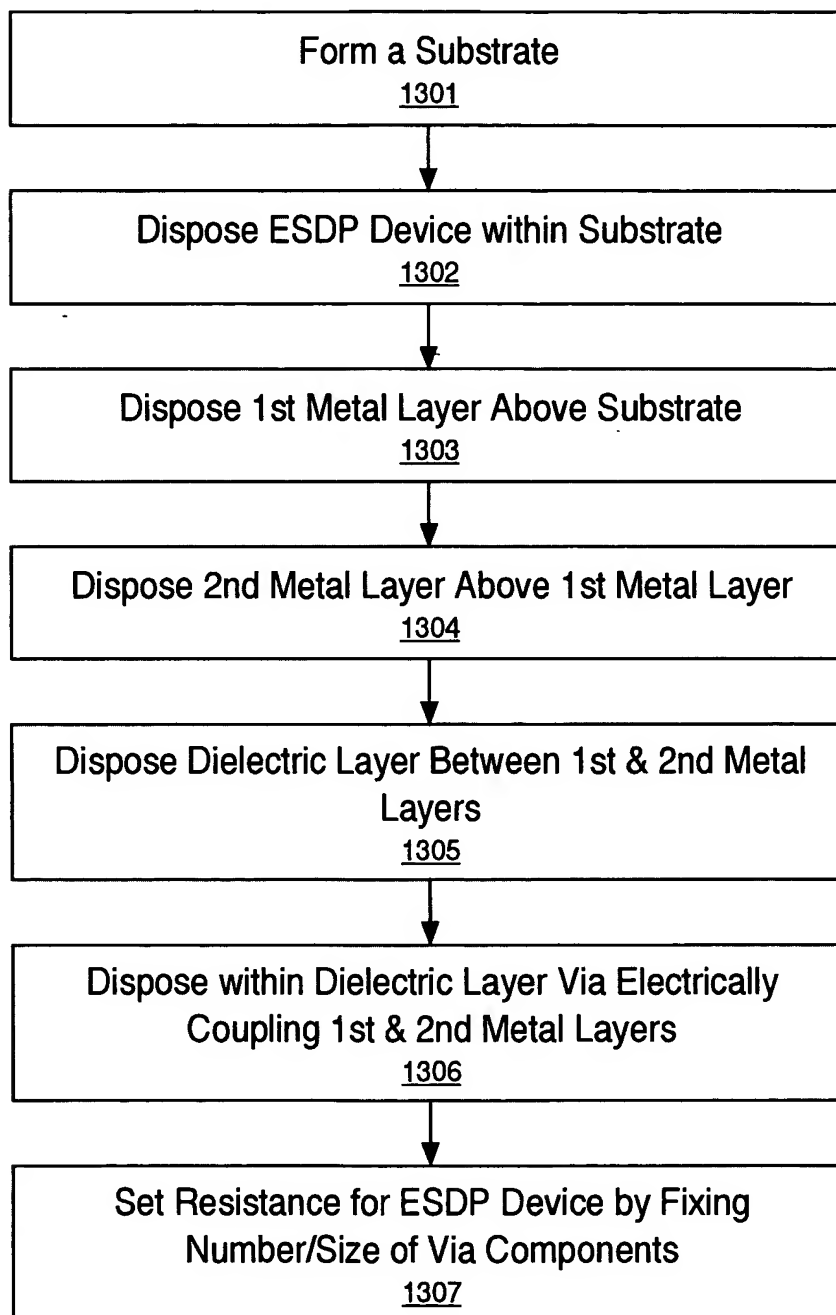


Fig. 13